CLAIMS

We claim:

1. A method of forming an integrated chip package, comprising the steps of:

providing a first substrate and a second substrate, each having conductive pads thereon;

applying a mask to at least one of the first and second substrates, wherein the mask has a plurality of non-circular openings having a first dimension and a second dimension, such that the conductive pads are not covered by the mask in the direction of the first dimension and partially covered by the mask in the direction of the second dimension; and

providing a reflowable material between the conductive pads of the first and second substrates.

2. The method of claim 1, wherein the first dimension of the elongated non-circular openings is greater than the second dimension of the non-circular openings.

3. The method of claim 1, wherein the first dimension of the non-circular openings is selectively oriented in the direction of highest stress for each interconnection formed from the reflowable material within the integrated chip package.

4. The method of claim 1, wherein the non-circular openings of the mask are elliptical.

5. The method of claim 1, wherein the conductive pads are circular.

6. The method of claim 5, wherein the conductive pads are copper.

7. The method of claim 1, wherein the mask comprises a non-wettable material.

8. The method of claim 7, wherein the mask comprises an epoxy.

9. The method of claim 1, wherein the first substrate is a chip carrier.

10. The method of claim 1, wherein the second substrate is a printed circuit board.

11. The method of claim 1, wherein the reflowable material is solder.

12. The method of claim 1, wherein a plurality of traces are mounted between the non-circular openings of the mask.

13. The method of claim 1, wherein the integrated chip package is a Ball Grid Array package.

14. An integrated chip package comprising:

a first substrate and a second substrate, wherein at least one of the first and second substrates includes a plurality of partially captured pads; and

a plurality of interconnections between the first and second substrates.

15. The integrated chip package of claim 14, wherein the plurality of partially captured pads are formed by a mask having elongated non-circular mask openings.

16. The integrated chip package of claim 15, wherein the elongated non-circular mask openings have a first dimension and a second dimension.

17. The integrated chip package of claim 16, wherein the first dimension of the elongated non-circular mask openings is greater than the second dimension of the elongated non-circular mask openings.

18. The integrated chip package of claim 16, wherein the first dimension of the elongated non-circular mask openings is selectively oriented on the substrate in the direction of highest stress within each interconnection.

19. The integrated chip package of claim 14, wherein the interconnections have a combination of mask-defined and pad-defined solder joint profiles.

20. A substrate having a plurality of conductive pads and a mask thereon, wherein the mask has a plurality of openings having a first dimension larger than the conductive pad, and a second dimension smaller than the conductive pad.

21. The substrate of claim 20, wherein the conductive pads are circular.

22. The substrate of claim 20 wherein the first dimension of the openings is greater than the second dimension of the openings.

23. The substrate of claim 22, wherein the first dimension of the openings is selectively oriented in the direction of highest stress within a plurality of interconnections formed within the openings of the substrate.

24. An integrated circuit mask having a plurality of elongated non-circular openings therein, wherein the openings have a first dimension greater than a second dimension, such that the first dimension of the openings coincides with the direction of the highest stress within the integrated circuit.

25. The integrated circuit mask of claim 24, wherein the mask comprises a non-wettable material.

26. An integrated circuit interconnection, wherein the interconnection is mask-defined in a first direction and pad-defined in a second direction.